MULTIMEDIA UNIVERSITY

STUDENT ID NO

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# MULTIMEDIA UNIVERSITY

# FINAL EXAMINATION

**TRIMESTER 3, 2021/2022**

## EEE1046 – ELECTRONICS III

( All sections / Groups )

11 August 2022
9:00 AM – 11:00 AM
( 2 Hours )

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**INSTRUCTIONS TO STUDENTS**

1. This Question paper consists of 8 pages (including the cover page) with 4 Questions only.

2. Attempt **ALL** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please write all your answers in the Answer Booklet provided.

## Question 1

(a) Identify **TWO** statements that are **FALSE** about operational amplifier (op-amp):

A. Infinite common-mode rejection of an ideal op-amp amplifies the voltage difference between the non-inverting and inverting inputs.

B. Negative feedback is the process whereby a portion of the output signal of an amplifier is returned to its non-inverting input.

C. A summing amplifier can have any number of inputs.

D. When a triangular waveform is applied to the input of a differentiator circuit, the output is an inverted triangular waveform.

[2 marks]

(b) An ideal non-inverting amplifier can be constructed using an operational amplifier (op-amp) and an external negative feedback circuit.

(i) Draw the schematic diagram of an ideal non-inverting op-amp circuit. In your sketch, clearly indicate the following:

- Series input resistor $R_I$ ;
- Feedback resistor $R_F$ ;
- Input voltage $V_{IN}$ ; and
- Output voltage $V_{OUT}$ . [3 marks]

(ii) Based on your sketch in Part (b)(ii), derive the equation for the closed loop voltage gain $A_{CL}$ of the ideal non-inverting amplifier. [4 marks]

(iii) Suggest suitable resistor values for $R_I$ and $R_F$ to have a closed-loop voltage gain $A_{CL} = 48$. [2 marks]

(c) Figure Q1.1 depicts the schematic diagram of an ideal op-amp differentiator circuit with an input signal $V_I$ as shown in Figure Q1.2.

(i) Derive the expression for the output voltage $V_O$ of the ideal differentiator. [4 marks]

(ii) The differentiator has $C_1 = 220$ pF and $R_F = 33$ kΩ. Determine the output voltage and draw the graph of the output waveform with respect to the input signal. [7 marks]

(iii) Explain why the ideal differentiator circuit is susceptible to electrical noise at high frequencies. [3 marks]

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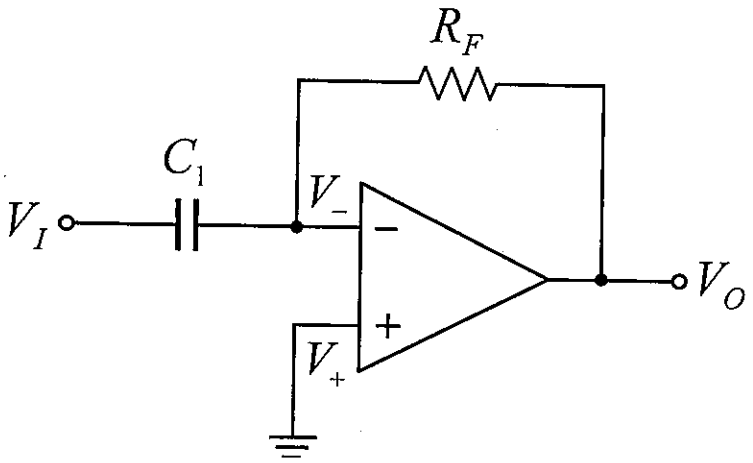


Figure Q1.1

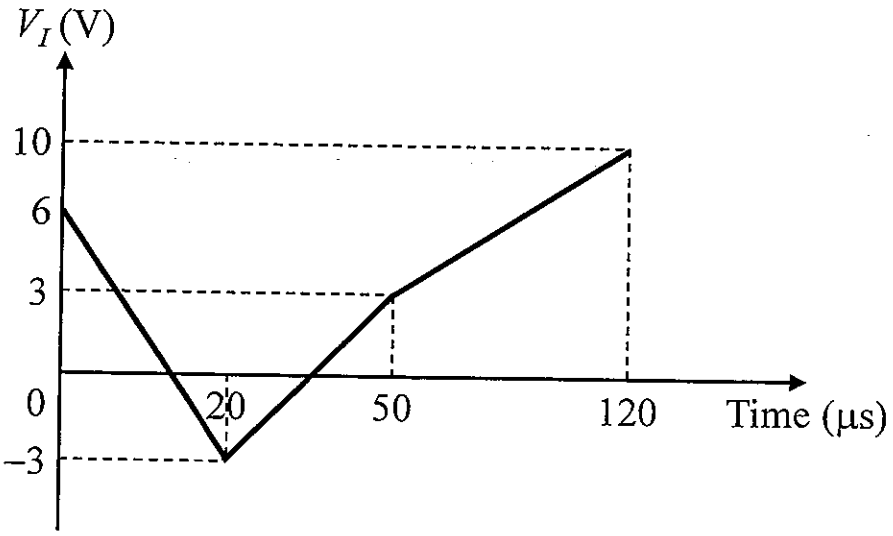


Figure Q1.2

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## Question 2

(a) Explain the **THREE** main stages which form the internal structure of an integrated circuit (IC) op-amp. [5 marks]

(b) An LM741 op-amp is used to construct an inverting amplifier with a closed-loop voltage gain $A_{CL} = -(R_F / R_1)$, where $R_1 = 10$ kΩ and $R_F = 220$ kΩ. The op-amp has an input offset voltage $V_{IO} = 5$ mV, input bias current $I_B = 250$ nA, and input offset current $I_{IO} = 120$ nA.

(i) The effect of the input bias current $I_B$ can be minimized by placing a bias-compensation resistance $R_X$ at the non-inverting input of the op-amp. Derive the expression for $R_X$. [7 marks]

(ii) Calculate the value of $R_X$. [2 marks]

(iii) Determine the total output offset voltage $V_{OO}$. [4 marks]

(c) Consider a non-inverting amplifier circuit, with an input series resistor $R_1 = 10$ kΩ and feedback resistor $R_F = 100$ kΩ. The op-amp has a unity-gain bandwidth $f_T = 15$ MHz and slew rate of 1.25 V/μs, and is biased at ±15 V. The signal bandwidth is 50 kHz.

(i) Determine the maximum closed-loop voltage gain. [2 marks]

(ii) Find the maximum peak output voltage. [2 marks]

(iii) Sketch the frequency response of the non-inverting amplifier, clearly indicating the following:

- Maximum closed-loop gain $A_{cl(max)}$ ;
- Closed-loop critical frequency $f_{c(cl)}$ ; and
- Unity-gain bandwidth $f_T$ . [3 marks]

**Continued .....**

## Question 3

(a) TWO (2) transistor regulator circuits are shown in Figure Q3(a) Both regulators are used to provide a regulated output voltage, $V_o$ of 9 V. The nominal source voltages of the unregulated power supply, $V_s$ are 15 V respectively. Both Zener diodes have knee current, $I_{ZK}$ of 10 mA, both transistors have DC current gain, $h_{FE}$ of 100 and base-emitter voltages, $V_{BE}$ of 0.7V. The load resistor, $R_L$ is 100 Ω.

[Hint: For regulator 1, $I_B = I_{ZK}$, and for regulator 2, $I_B \approx \frac{I_L}{h_{FE}}$ where $I_L$ is current at the load]

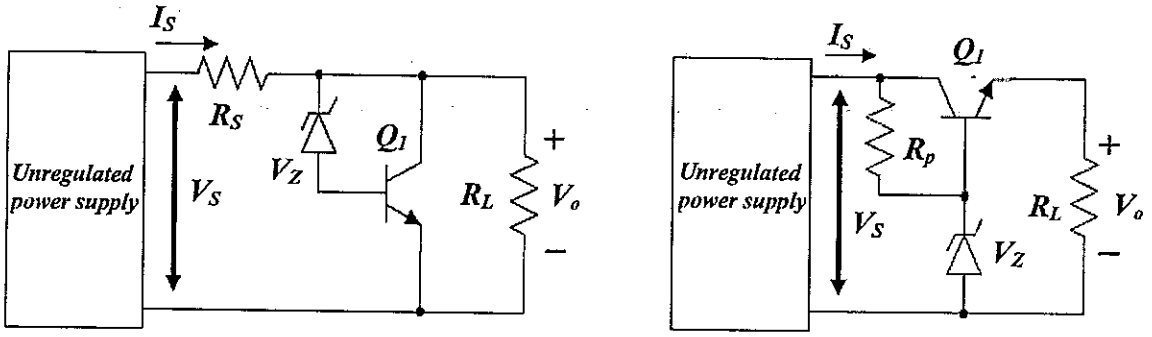


Figure Q3(a)

(i) Name the type of regulators used in Figure 3(a). Which regulator is suited to low voltages application?

[3 marks]

(ii) Determine the voltage drop across the Zener diode, $V_Z$ for both circuits.

[2 marks]

(iii) Calculate the current flow from the unregulated power supply, $I_S$ for both circuits

[3+3 marks]

(iv) Compare the efficiency for both regulators. Which regulator has the higher efficiency? Explain briefly your answer.

[5 marks]

(b) A phase-shift oscillator circuit is shown in Figure Q3(b), where its feedback voltage gain, $\beta$ is given as:

$$\beta = \frac{R^3}{R^3 - 5R\left(\frac{1}{\omega C}\right)^2 + j\left[\left(\frac{1}{\omega C}\right)^3 - \frac{6R^2}{\omega C}\right]}$$

Assume the op-amp is ideal.

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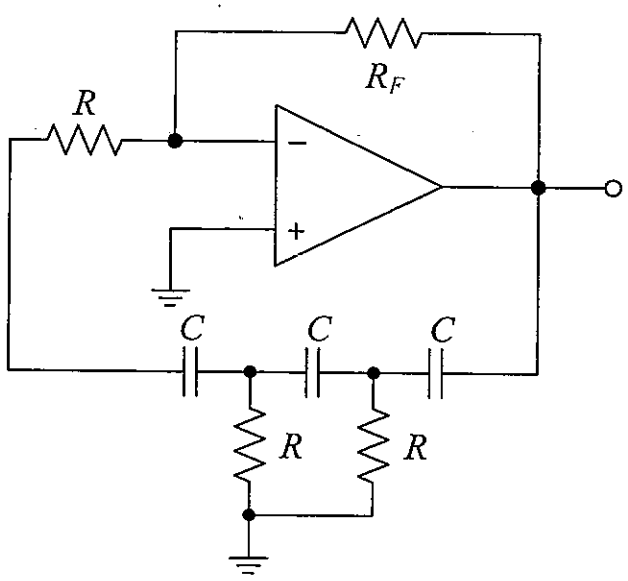


Figure Q3(b)

(i) Determine $\beta$ and the required amplifier gain, $A$ for oscillation.
[ Hint: Assume both β and $A$ are real in this expression]

[5 marks]

(ii) Determine the value of $R$ and $C$ for the circuit with oscillation frequency, $f_o = 800$ Hz, and $R_F = 100$ kΩ. The voltage gain magnitude of the amplifier should be 3% higher than its minimum value for oscillation.

[4 marks]

## Question 4

(a) A filter circuit with two input resistors, $R_1$ and $R_2$, two capacitors, $C_1$ and $C_2$, two ground resistors, $R_3$ and $R_4$, a feedback resistor, $R_5$, and a voltage gain response, $A_v$ (in dB) from approximately DC to 600 kHz, is shown in Figure Q4(a). A three-tone sinusoidal signal, $Vin(t)$ with frequencies of $f_1 = 50$ kHz, $f_2 = 400$ kHz and $f_3 = 500$ kHz is applied at the input and it is given as:

$$V_{in}(t) = 10\cos(2\pi f_1 t) + 20\cos(2\pi f_2 t) + 20\cos(2\pi f_3 t)$$

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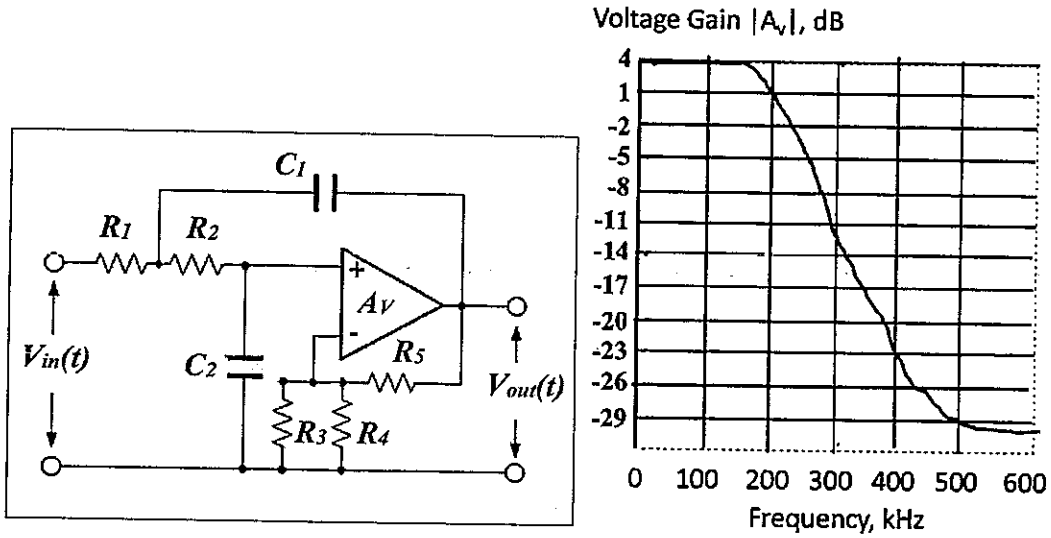


**Figure Q4(a)**

(i) What type and order of the filter is shown in the above circuit? How many poles in this filter?

[3 marks]

(ii) Determine the gain (at pass band), 3 dB cut-off frequency, pass band frequencies and stop band frequencies of the filter.

[4 marks]

(iii) Assume equal values for the ground resistors, $R_3 = R_4 = 10$ kΩ, determine the feedback resistor, $R_5$ for the above circuit.

[4 marks]

(iv) Assume equal values for the input resistors and capacitors, $R_1 = R_2 = R$ and $C_1 = C_2 = 1$ nF, determine the input resistors, $R_1$ and $R_2$ for the above circuit.

[2 marks]

(v) Calculate the damping factor, α for this circuit. What type of filter for this circuit? Is it Butterworth, Bessel or Chebyshev?

[2 marks]

(vi) Determine the output sinusoidal signal, $V_{out}$.

[4 marks]

(b) A non-inverting comparator circuit with an input signal, $V_{IN}$ is shown in Figure Q4(b). Two 1 kΩ resistors are connected as potential divider network across the supply voltage, $V_{CC}$ of 6V, to produce a fixed reference voltage, $V_{REF}$.

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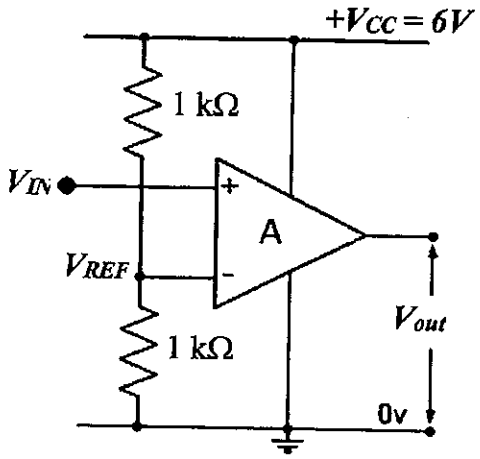


**Figure 4(b)**

(i) Explain briefly the function of comparator in non-linear application. State TWO (2) applications of comparator in electronics devices.

[4 marks]

(ii) Determine the fixed reference voltage, $V_{REF}$.

[2 marks]

**End of paper**